REMARKS

Claims 34-49 were renumbered by the Examiner as claims 21-36. The claim dependencies have been amended to reflect this renumbering. Many of the claims have been amended to put them into a better form. Claims 1-20 have been canceled from the parent case.

Double Patenting Rejection

Claims 21-36 were rejected under the judicially created doctrine of obviousness-type double patenting. Applicants include a terminal disclaimer and request withdrawal of this rejection.

Objection to the Drawings

The Drawings were objected to. In particular, the numeral "461" in Fig. 4 should be "61." A Replacement Drawing Sheet reflecting this change is submitted for the Examiner's approval.

Objections to the Specification

The specification was objected to because of a number of informalities. These have been corrected as requested by the Examiner.

Objections to the Claims

Claims 21, 26, 29, and 34 were objected to because of the phrase "in responsive to said first instruction." It is respectfully submitted that claim 26 does not include this language. Claims 21, 29 and 34 have been amended to correct the informalities.

Rejections of the Claims under 35 U.S.C. § 112, Second Paragraph

Claims 24 and 25 were rejected under 35 U.S.C. § 112, second paragraph as failing to distinctly claim the present invention. Claim 24 has been amended in accordance with the Examiner's suggestion.

Rejections of the Claims under 35 U.S.C. §§ 102(e) and 103(a)

Claims 21-25 and 29-33 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,493,741 to Emer et al. ("Emer"). Claims 26-28 and 34-36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Emer.

In discussing the Emer reference, Applicants are making no admission that Emer has a filing date that predates the invention date of the present application.

Emer refers to the execution of a number of different instructions in a multi-threaded processor. In particular, the quiesce request instruction 117 is executed by a TPU (thread processing unit) and causes the TPU to enter into a quiesce mode. (See Col. 5, lines 62-67). As seen in Fig. 2, there are multiple thread processing units 101A ..N in a CPU 100.

Claim 21 recites that a first instruction can result in the pausing of processing of instructions from the first thread at a pipeline stage while processing instructions from a second thread at the pipeline stage of the processor. Claim 26 includes a similar limitation. Such a feature is neither taught nor suggested by Emer. In Emer, the entire thread processing unit is quiesced. If such a TPU includes pipeline stages (though none are described in Emer), then none of those pipeline stages would be processing instructions from a second thread as called for in these claims.

Claim 29 refers to a decode unit that is to determine whether a first instruction of a first thread is an instruction a first type and to pause processing of instruction of the first thread. Claim 34 includes a similar limitation. Such a feature is neither taught nor suggested by Emer.

In Emer, the execution of the quiesce request instruction 117 causes placing the TPU into a quiesce state. The Office Action states that some sort of decoding is required in Emer. Whether decoding occurs or not, however, there is nothing in Emer that describes a decode unit having the features that are recited in these claims.

Since features of the claims are neither taught nor suggested by Emer, reconsideration and withdrawal of the rejection of claims 21-36 under 35 U.S.C. §§ 102(e) and 103(a) is respectfully requested.

CONCLUSION

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,

Dated: 2/16/06

By: Shawn O'Dowd

Shawn W. O'Dowd
Reg. No. 34,687

KENYON & KENYON LLP
1500 K Street, N.W.
Washington, DC 20005
(202) 220-4200 telephone
(202) 220-4201 facsimile